# A Multiplexing Ripple Cancellation LED Driver With True Single-Stage Power Conversion and Flicker-Free Operation

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***Abstract*—Although a single-stage off-line power light-emitting diode (LED) driver can achieve low cost and high efficiency, the notorious double-line-frequency flicker issue with a single-stage LED driver limits its usage in high-quality lighting applications. To solve lighting flicker, as well as maintain a low cost and high efficiency, a multiplexing ripple cancellation (MRC) LED driver is proposed in this paper. One switching cycle is divided into two intervals. During the first interval, the proposed LED driver operates as a conventional LED driver that transfers energy from the ac input to LED output, performs power factor correction, and generates the main output voltage. The main output voltage has a double-line-frequency ripple like in a conventional design. During the second interval, the proposed LED driver transfers energy from the ac input again to generate an opposite ripple voltage to cancel the ripple voltage from the main output. In this way, the voltage across the LED load is a dc to achieve flicker-free LED driving performance. More than 99% of the output power goes through one-time power conversion, while less than 1% goes through two-time power conversion. A 7.5-W experimental prototype is built and tested to verify the design concept.**

***Index Terms*—Flicker-free operation, high power factor, multiplexing operation, off-line light-emitting diode (LED) driver, ripple cancellation.**

## I. Introduction

THE light-emitting diode (LED) offers much higher efficacy than any other lighting devices and is one of the most promising new lighting technologies. High-quality LED light devices are more durable and provide comparable, if not better, light quality as other types of lighting. It has the potential to completely overtake other traditional light technologies, especially in residential applications. The global LED lighting market reached US$ 26 billion in 2016 and is expected to reach US$ 54 billion by 2022, growing at a rate of around 13% between 2017 and 2022 [1].

The LED driver, a specially designed power supply to regulate LED current, is the key technology in LED lighting, which determines the overall efficiency, lighting quality as well as the reliability of an LED lighting device. EnergyStar requires any ac connected LED driver to achieve a power factor higher than 0.9 for commercial applications or 0.7 for residential applications when its rated output power is greater than 5 W [2]. IEC-61000-3-2 further imposes limitations on input current harmonics for lighting device with more than 75 W rated output power. Complying with these requirements imposes great challenges on designing an ac-connected LED driver. The ac input power of an LED driver is a sinusoid-like waveform with a double-line-frequency ripple. A significant portion of the double-line-frequency ripple energy is usually passed to the LED load when a single-stage LED driver is used, which produces lighting flicker. It is well documented that lighting flicker at double-line-frequency is very harmful to our health, resulting in both short- and long-term health concerns [2]. The situation is much better when a two-stage LED driver is used. A two-stage LED driver can minimize the LED load ripple energy to a negligible level, achieving the so-called flicker-free operation. However, a two-stage LED driver has a much higher component cost and lower efficiency, which is extremely undesirable in cost-sensitive, low-power applications, for example, in LED light bulbs applications.

A great deal of research has been conducted in an attempt to design an LED driver that maintains the high efficiency and low cost of a single-stage solution, which also achieves the flicker-free operation of a two-stage LED driver. The energy buffering technologies [4]–[7] have been proposed to balance energy difference between ac input and LED output with a bidirectional dc–dc converter. The two-stage integrated methods [8]–[11] have been proposed to share components between the first PFC stage and the second dc–dc stage, which can reduce the component cost. The harmonic input currents injection method [12]–[14] have been proposed to minimize the double-line-frequency imbalanced energy existing in a single-stage LED driver. Therefore, the ripple LED current is reduced to alleviate lighting flicker.

The ripple cancellation method is proposed in [15]–[20]. A ripple cancellation converter is used in the designs to

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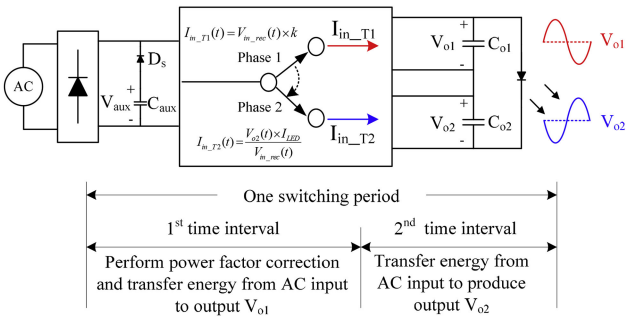


Fig. 1. Concept of the proposed MRC LED driver.

generate an opposite ripple voltage, which cancels the ripple voltage from the main output. As a result, a DC voltage is produced and applied to the LED load to achieve flicker-free LED driving performance. The greatest merits of this method are low component cost and high efficiency. The ripple cancellation converter processes only a small fraction of the total output power, which requires a minimal additional cost to implement and yields overall high efficiency. The energy-channeling LED driver is proposed in [20]. The input power is split into two portions, with the first major portion being transferred to the LED load and the second portion generating an opposite ripple voltage to achieve ripple cancellation. The great advantage of this solution is more than 98% of the output power go through one power conversion step, leading to an improved efficiency. One drawback of the energy-channeling LED driver is restricted operation. When a high power factor is achieved, the input power is a dc-biased sinusoidal waveform with a minimum value of zero. The energy available to sustain $V_{o2}$ is from the input power and it will not be enough when the input power becomes very small. Complex auxiliary circuitry is needed to maintain proper operation of the energy-channeling LED driver. A multiplexing ripple cancellation (MRC) LED driver is proposed in this paper. It is also a true single-stage LED driver with 99.5% output power being processed once. It operates drastically different from the energy-channeling LED driver to free itself from the aforementioned limitation. In the new LED driver, the task of performing power factor correction and sustaining output $V_{o2}$ are done in two separate intervals of one switching cycle. Therefore, sustaining the ripple cancellation voltage is independent of the power factor correction operation, and the aforementioned limitation in the energy-channeling LED driver is eliminated.

The remaining sections of this paper are organized as follows. Section II discusses the concept and operating principle of the proposed LED driver. Section III discusses the component voltage and current stresses. Section IV discusses the control strategy of the LED driver. Section V discusses the design considerations and an example design procedure. Different LED driving technologies are compared in Section VI. The experimental results of the proposed LED driver are presented in Section VI. Finally, the paper is concluded in Section VII.

## II. Concept and Operating Principle

Fig. 1 shows the operation concept of the proposed MRC LED driver. It operates in time multiplexing manner, with one switching cycle being divided into two intervals, namely, interval I and interval II. During the time interval I, the power stage of the conceptual LED driver operates as a power factor correction (PFC) converter. Energy is transferred from the ac input to the main output $V_{o1}$ and power factor correction is performed. During interval II, it operates as a ripple cancellation converter. The energy used to maintain $V_{o2}$ is also from the ac input. The energy transferred from the ac input to both output $V_{o1}$ and $V_{o2}$ is done using a single-stage power conversion, which helps maintain a high efficiency comparable to a conventional single-stage LED driver. Although the proposed LED driver is validated with a 7.5-W experimental prototype, the same concept can be expandable for higher output power designs.

On the other side, the proposed LED driver has its own limitation, which is explained as follows. The current drawn from the ac input (after input bridge rectifier) during the interval I operation is named as $I_{in\_T1}$ and the current drawn from the ac input during the interval II operation is named as $I_{In\_T2}$. $I_{in\_T1}$ follows the input voltage to achieve the power factor correction and can be expressed as

$$I_{in\_T1}(t) = V_{in\_rec}(t) \times k \tag{1}$$

where $k$ is a constant coefficient between the input voltage and $I_{in\_T1}$ in (1). During interval II, the power needed to maintain $V_{o2}$ is also supplied from the ac input. Therefore, $I_{in\_T2}$ can be expressed as

$$I_{in\_T2}(t) = \frac{V_{o2}(t) \times I_{\mathrm{LED}}}{V_{in\_rec}(t)}. \tag{2}$$

As indicated by (2), $I_{in\_T2}$ does not follow the input voltage. Therefore, the overall ac input current is not an ideal sinusoidal waveform. To minimize the harmonic currents from $I_{in\_T2}$, it should be kept as small as possible, which can be achieved by reducing the output voltage $V_{o2}$.

In addition, (2) also indicates that $I_{in\_T2}(\mathrm{t})$ will approach infinity when $V_{\mathrm{in}}(t)$ drops to zero. Therefore, to curb the ac input current during the ac input voltage zero-crossing, the input voltage should be limited to a minimal level instead of dropping to zero. A voltage source $V_{\mathrm{aux}}$ can be added after the bridge rectifier and the minimum input voltage after input rectifier becomes

$$V_{in\_rec\_\min} = V_{\mathrm{aux}}. \tag{3}$$

$V_{\mathrm{aux}}$ can be separated from the input bus with a diode $D_s$ that is shown in Fig. 1. When $|V_{in}(t)| > V_{\mathrm{aux}}$, the diode $D_s$ is reversely biased and the energy is taken from the ac input. When $|V_{in}(t)| < V_{\mathrm{aux}}$, the bridge rectifier diodes are reversely biased, during which $D_s$ conducts current and the energy is supplied by $V_{\mathrm{aux}}$. The ac input current becomes zero during this period. It should note that, as an autonomous system, $V_{\mathrm{aux}}$ is also generated by the power circuit of the LED driver. $V_{\mathrm{aux}}$ can be generated in flyback mode energy transfer fashion. By addition of another winding in the inductor and orienting it in the same way as that of the main winding $N_1$, a voltage can be developed on the new winding when the diode $D_1$ is conducting, and this voltage is a scaled reflection of the output $V_{o1}$, with the value determined by the turns ratio between $N_1$ and the new winding.

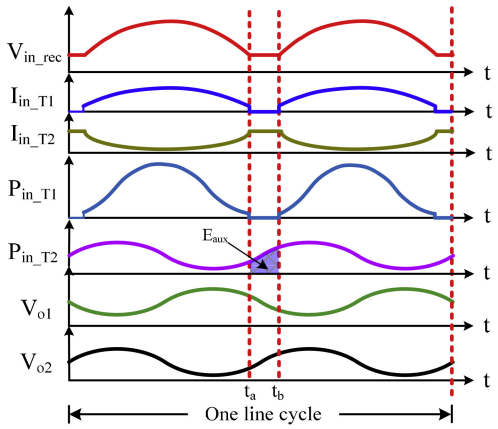


Fig. 2. Critical line cycle waveforms of the proposed MRC LED driver.

A dc voltage can be generated by rectifying the winding voltage with a diode.

Also, it can be understood that the energy supplied by $V_{\rm aux}$ goes through two power conversion steps. First, the energy is transferred from the ac input to $V_{\rm aux}$. Second, the energy is transferred from $V_{\rm aux}$ to the LED load. As mentioned, one key feature of the proposed MRC LED driver is to achieve single-stage power conversion. The following measure is adopted to minimize the amount of energy going through two times power conversion—once $V_{\rm aux}$ kicks in to supply the energy, the interval I operation is temporary disabled. Therefore, $V_{\rm aux}$ only supplies energy to $V_{o2}$ through the interval II operation, which is typically less than 1% of the total energy delivered to the LED load, as will be analyzed later.

The key line cycle waveforms of the proposed MRC LED driver are shown in Fig. 2. When $|V_{in}| > V_{\rm aux}$, the time interval I, the ac input current $I_{in\_T1}$ follows the input voltage. When $|V_{in}| < V_{\rm aux}$, $I_{in\_T1}$ is zero as the time interval I operation is disabled under this condition. The current $I_{in\_T2}$ is provided by the voltage source $V_{\rm aux}$. The time interval I input power $P_{in\_T1}$ is a dc-biased sinusoidal waveform with a zero-power region when $|V_{in}| < V_{\rm aux}$. Similar to a conventional PFC, the ripple power of $P_{\rm ph1}$ produces a ripple voltage on the main output $V_{o1}$ and the ripple voltage of $V_{o1}$ is approximately 90° lagging the double-line-frequency ripple of $P_{in\_T1}$. To achieve cancellation, the double-line-frequency ripple voltage of $V_{o2}$ is made to be opposite to that of $V_{o1}$. The amount of energy transferred by $V_{\rm aux}$ can be expressed as

$$E_{\rm aux} = \int_{t_a}^{t_b} V_{o2}(t) \times I_{\rm LED} \tag{4}$$

where $E_{\rm aux}$ represents the energy provided by $V_{\rm aux}$ in a half line cycle and $t_a$ and $t_b$ represent the beginning and the end points when $|V_{in}| < V_{\rm aux}$. Since the output $V_{o2}$ stays around the average value when $|V_{in}| < V_{\rm aux}$, (4) can be further simplified as

$$E_{\rm aux} \approx V_{o2\_avg} \times I_{\rm LED} \times (t_b - t_a). \tag{5}$$

The time $(t_b - t_a)$ can be calculated as

$$t_b - t_a = \frac{\arcsin\left(\frac{V_{\rm aux}}{V_{in\_pk}}\right)}{\pi} \times T_{\rm line}. \tag{6}$$

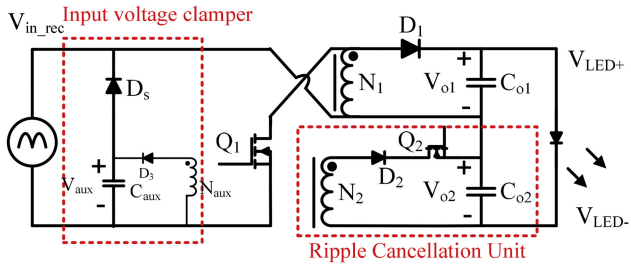


Fig. 3. Circuit implementation of the MRC LED driver based on the buck–boost topology.

Combining (5) and (6) yields

$$E_{\rm aux} \approx V_{o2\_avg} \times I_{\rm LED} \times \frac{\arcsin\left(\frac{V_{\rm aux}}{V_{in\_pk}}\right)}{\pi} \times T_{\rm line}. \tag{7}$$

$(t_b–t_a)$ is calculated to be 1.03 ms when $V_{\rm aux} = 30$ V and $V_{in} = 110$ Vrms. Using $V_{o2\_avg} = 2.5$ V and $I_{\rm LED} = 0.15$ A, $E_{\rm aux}$ is calculated to be 2.5 V × 0.15 A × 1.03 ms = 0.39 mJ. The total energy delivered to the LED load in a half line cycle is 7.5 W × $(2f_{\rm line}) = 62.5$ mJ. Therefore, only 0.6% of the total energy is processed twice and 99.4% of the energy goes through the single-stage power conversion. Thus, the proposed LED driver can be reasonably said to operate as a single-stage LED driver.

The limitation of the proposed MRC LED driver, as discussed earlier, is the harmonic currents introduced by the time interval II operation and by the ac input current zero-crossing distortion. More discussion will be presented in Section V to investigate the limitation of the proposed MRC LED driver and a design guideline to reduce harmonics current will be provided to comply with IEC-61000-3-2 for designs with greater than 75 W output power.

Fig. 3 shows a buck–boost topology-based implementation of the MRC LED driver. The same concept can be implemented with other current-fed topologies, such as flyback and boost. Compared to a conventional buck–boost LED driver, the proposed MRC LED driver contains an additional ripple cancellation unit (RCU) and the input voltage clamp unit, which are both highlighted in Fig. 3. The RCU is active during the interval II operation, through which an opposite ripple voltage is produced. It will be discussed in Section IV that the voltage stresses of $D_2$ and $Q_2$ are very low (around 20 V) so that low voltage rating devices can be used to maintain an overall low cost. As the energy processed by $V_{\rm aux}$ is around 0.5% of the overall output power, very low-cost components can be used to generate $V_{\rm aux}$, which will not contribute too much cost. The same is also true with $D_s$, which provides current flow path when $V_{\rm aux}$ provides energy. On the contrary, the second-stage dc–dc converter needs to process 100% of output power. Therefore, the cost to implement the second-stage dc–dc converter in a two-stage design is much greater. In addition, the proposed LED driver does not need an extra inductor to generate the ripple cancellation voltage, which also helps to save cost.

To facilitate a better understanding of the structure of the proposed MRC LED driver, its equivalent circuits during the

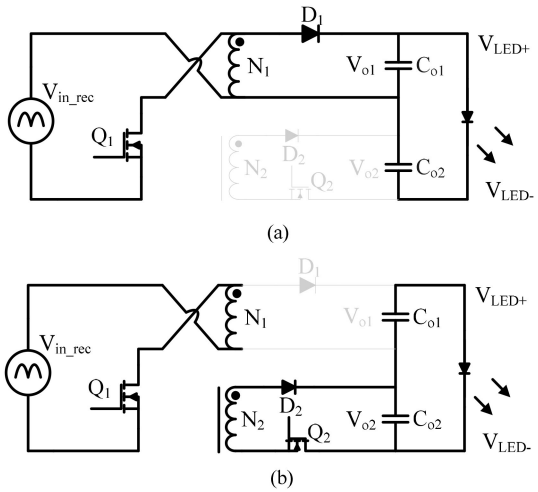


Fig. 4. Equivalent circuits of the MRC LED driver. (a) Interval I circuit. (b) Interval II circuit.

interval I and the interval II operations are shown in Fig. 4. During the interval I operation, the equivalent circuit is operated as an independent buck–boost PFC converter. During the interval II operation, the equivalent circuit is operated as an independent flyback converter. Fig. 5 shows one switching cycle operation of the MRC LED driver. The time interval I operation is further divided into two time intervals [$t_0$–$t_1$] and [$t_1$–$t_2$], and the time interval II operation is further divided into intervals [$t_2$–$t_3$] and [$t_3$–$t_4$]. Note that the voltage $V_{\rm aux}$ and $D_3$ are not shown in Figs. 4 and 5 for succinctness.

The critical switching waveforms in one switching cycle is shown in Fig. 6. The following brief analysis explains how power factor correction is performed during the time interval I operation. The switching current starts from zero at the beginning of the time interval I operation. The ON time of the interval I operation [$t_0$–$t_1$] is a constant in a half line cycle. The interval II operation will not start until the switching current $I_{D1}$ drops to zero. At the end of time interval II operation, switching current $I_{D2}$ also drops to zero. The switching period is constant in every switching cycle. The detailed switching operation in each time interval will be discussed as follows.

### A. Time [$t_0$–$t_1$]

A switching cycle starts at time $t_0$ when MOSFET $Q_1$ is turned ON. The inductor is charged by the rectified ac input. The switching current, in winding $N_1$, starts rising from zero and increases linearly with the turn on time. The switching current in winding $N_1$ (and $Q_1$) peaks at time $t_1$ right before $Q_1$ is turned OFF and can be expressed as

$$I_{Q_1\_t_1} = \frac{V_{\rm in} \times (t_1 - t_0)}{L_{N1}}. \tag{8}$$

The average current drawn from the ac input during time interval I operation can be expressed as

$$I_{in\_T1\_avg} = \frac{I_{Q1\_t_1} \times (t_1 - t_0)}{2T_s} \tag{9}$$

where $I_{in\_T1\_avg}$ represents the average input current in a switching cycle during the interval I operation. Further combining (8) and (9) yields

$$I_{in\_T1\_avg} = \frac{V_{\rm in} \times (t_1 - t_0)^2}{2 \times T_s \times L_{N1}}. \tag{10}$$

As both the terms ($t_1$–$t_0$) and $T_s$ are constant in a half line cycle, $I_{in\_T1\_avg}$ is therefore proportional to the input voltage. Because of the opposite winding orientation between $N_1$ and $N_2$, both diodes $D_1$ and $D_2$ are reversely biased and there is no current in winding $N_2$. The body diode of MOSFET $Q_2$ is forward biased. The voltage stresses on $D_1$ and $D_2$ during this time interval can be expressed as

$$V_{D_1[t_0-t_1]} = V_{o1} + V_{\rm in} \tag{11}$$

$$V_{D_2[t_0-t_1]} = V_{o2} + V_{\rm in} \times \frac{N_2}{N_1}. \tag{12}$$

### B. Time [$t_1$–$t_2$]

As MOSFET $Q_1$ is turned OFF at time $t_1$, the magnetic current in winding $N_1$ is forced to conduct in diode $D_1$. The voltage across winding $N_1$ is clamped to be the same as the output $V_{o1}$ (ignoring the forward voltage drop of diode $D_1$). The voltage across MOSFET $Q_1$ is the sum of the input voltage and the output voltage $V_{o1}$ and is expressed as

$$V_{Q_1[t_1-t_2]} = V_{\rm in} + V_{o1}. \tag{13}$$

During this time interval, the energy stored in the inductor is transferred to the output $V_{o1}$. The magnetic current in winding $N_1$ starts decreasing at time $t_1$ and becomes zero at time $t_2$, which ends the interval I operation. One should note that during this time interval, the voltage on winding $N_2$ $V_{N2[t1-t2]}$ is designed to be higher than $V_{o2}$ as shown

$$V_{N_2[t_1-t_2]} = V_{o1} \times \frac{N_2}{N_1} > V_{o2}. \tag{14}$$

Therefore, the diode $D_2$ is forward biased while the body diode of $Q_2$ is reversely biased. The voltage across the drain to source terminals of $Q_2$ can be expressed as

$$V_{Q_2[t_1-t_2]} = V_{N_2[t_1-t_2]} - V_{o2} = V_{o1} \times \frac{N_2}{N_1} - V_{o2}. \tag{15}$$

### C. Time [$t_2$–$t_3$]

The time interval II operation starts at time $t_2$ and MOSFET $Q_1$ is turned ON again. The voltage stresses on these power components are the same as they are during the time interval [$t_0$–$t_1$]. The inductor current in MOSFET $Q_1$ peaks at $t_3$ again before $Q_1$ is turned OFF. The switching current in $Q_1$ at $t_3$ is expressed as

$$I_{Q_1\_t_3} = \frac{V_{\rm in} \times (t_3 - t_2)}{L_{N1}}. \tag{16}$$

MOSFET $Q_2$ is designed to be turned ON at $t_2$. Theoretically, MOSFET $Q_2$ can be turned ON anywhere within [$t_2$–$t_3$] without affecting the expected operation.

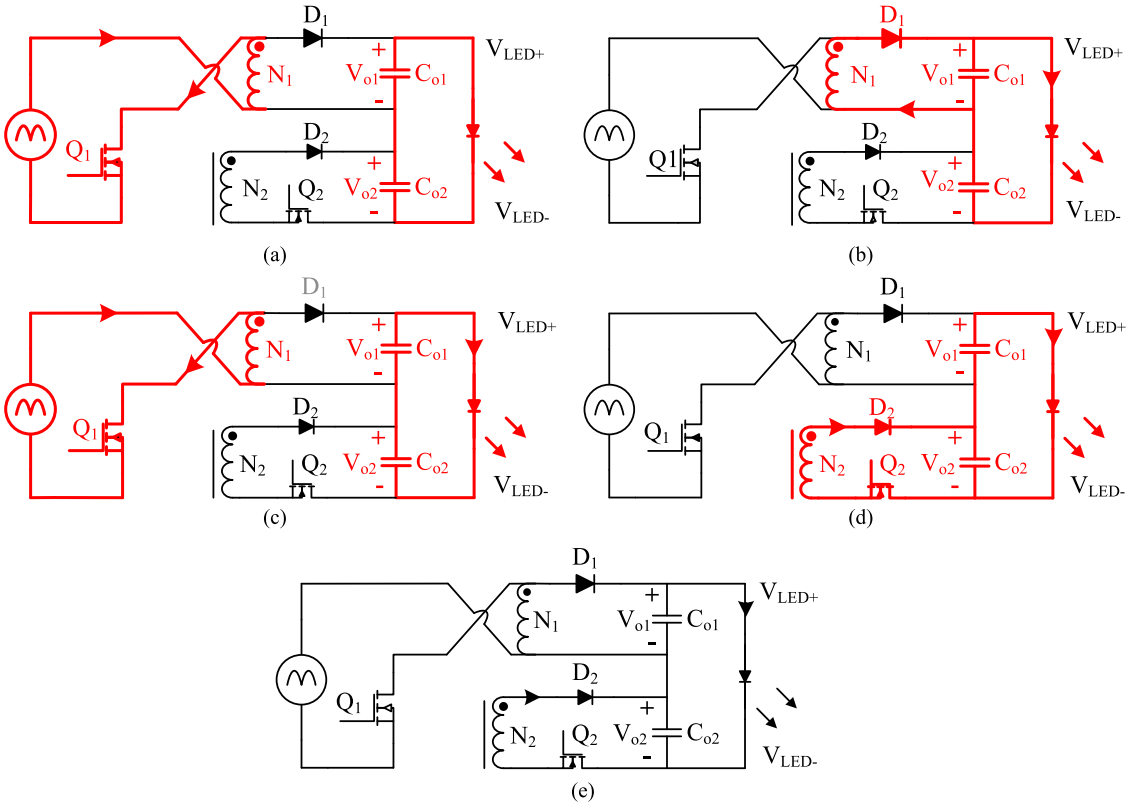


Fig. 5. One switching cycle operation of the proposed MRC LED driver. (a) $[t_0 - t_1]$. (b) $[t_1 - t_2]$. (c) $[t_2 - t_3]$. (d) $[t_3 - t_4]$. (e) $[t_4 - t_5]$.

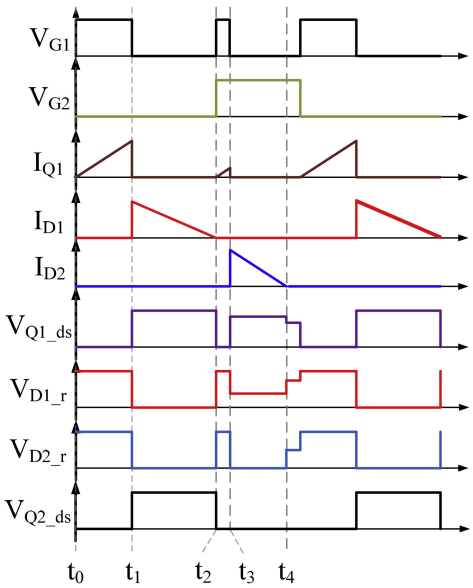


Fig. 6. Key switching current waveforms of the proposed MRC LED driver.

### D. Time $[t_3$–$t_4]$

When MOSFET $Q_1$ is turned OFF at $t_3$, the magnetic inductor current needs to find another path to continue the current flow. As $Q_2$ is already on, both winding $N_1$ and $N_2$ provide current flowing paths. The turns ratio $N_1$:$N_2$ in the proposed design forces the magnetic current to continue flowing in the winding $N_2$ and the explanation is as follows. If the magnetic current conducts in winding $N_2$, the voltage across the winding $N_2$ is clamped at $V_{o2}$ (with ignoring the forward voltage drop of $D_2$). The voltage reflected on the winding $N_1$ becomes

$$V_{N_1[t_3-t_4]} = V_{o2} \times \frac{N_2}{N_1}. \tag{17}$$

Combining (14) and (17) yields

$$V_{N_1[t_3-t_4]} < V_{o1}. \tag{18}$$

Equation (18) indicates that the voltage potential at the anode of $D_1$ is smaller than the voltage potential at the cathode of $D_1$. Therefore, the diode $D_1$ is reversely biased. Therefore, the aforementioned assumption is valid and the magnetic current only conducts in winding $N_2$ during $[t_3$–$t_4]$. The inductor releases the stored energy to the output $V_{o2}$ during the time interval $[t_3$–$t_4]$. The magnetic current in winding $N_2$ starts decreasing from $t_3$ and it drops to zero at time $t_4$, which ends the time interval II operation. There is a voltage falling on MOSFET $Q_1$ again, which can be expressed as

$$V_{Q_1[t_3-t_4]} = V_{\text{in}} + V_{o2} \times \frac{N_1}{N_2}. \tag{19}$$

### E. Time $[t_4$–$t_5]$

There is a small time interval $[t_4$–$t_5]$ to maintain the DCM operation. There is no active energy transfer during this time interval and the magnetic current in the inductor remains zero.

TABLE I
MRC LED DRIVER COMPONENT VOLTAGE STRESSES

| | $Q_1$ | $D_1$ | $Q_2$ | $D_2$ |
|---|---|---|---|---|
| $[t_0\text{-}t_1]$ | 0 | $V_{in}+V_{o1}$ | 0 | $V_{o2}+V_{in}\times\frac{N_2}{N_1}$ |
| $[t_1\text{-}t_2]$ | $V_{in}+V_{o1}$ | 0 | $V_{o1}\times\frac{N_2}{N_1}-V_{o2}$ | 0 |
| $[t_2\text{-}t_3]$ | 0 | $V_{in}+V_{o1}$ | 0 | $V_{o2}+V_{in}\times\frac{N_2}{N_1}$ |
| $[t_3\text{-}t_4]$ | $V_{in}+V_{o2}\times\frac{N_1}{N_2}$ | $V_{o1}-V_{o2}\times\frac{N_1}{N_2}$ | 0 | 0 |
| Max | $V_{in}+V_{o1}$ | $V_{in}+V_{o1}$ | $V_{o1}\times\frac{N_2}{N_1}-V_{o2}$ | $V_{o2}+V_{in}\times\frac{N_2}{N_1}$ |

TABLE II
MRC LEDS DRIVER COMPONENTS CURRENT STRESSES

| | $Q_1$ | $D_1$ |
|---|---|---|
| At $t_1$ | $\frac{V_{in}\times(t_1-t_0)}{L_{N1}}$ | $\frac{V_{in}\times(t_1-t_0)}{L_{N1}}$ |
| At $t_3$ | $\frac{V_{in}\times(t_2-t_3)}{L_{N1}}$ | 0 |
| Max | $Max\left\{\frac{V_{in}\times(t_1-t_0)}{L_{N1}},\frac{V_{in}\times(t_2-t_3)}{L_{N1}}\right\}$ | $\frac{V_{in}\times(t_1-t_0)}{L_{N1}}$ |
| | $Q_2$ | $D_2$ |
| At $t_3$ | $\frac{V_{in}\times(t_2-t_3)}{L_{N1}}\times\frac{N_1}{N_2}$ | $\frac{V_{in}\times(t_2-t_3)}{L_{N1}}\times\frac{N_1}{N_2}$ |
| Max | $Max\left\{\frac{V_{in}\times(t_1-t_0)}{L_{N1}},\frac{V_{in}\times(t_2-t_3)}{L_{N1}}\times\frac{N_1}{N_2}\right\}$ | $\frac{V_{in}\times(t_2-t_3)}{L_{N1}}\times\frac{N_1}{N_2}$ |

## III. VOLTAGE AND CURRENT STRESSES ANALYSIS

As the switching operation has been discussed, the maximum voltage stress of each component in one switching cycle is summarized in Table I.

The maximum voltage across the drain and the source terminals of $Q_1$ and the reverse voltage across the diode $D_1$ in a half line cycle occur when the input voltage reaches the maximum in a half line cycle. Therefore, the maximum voltage stresses can be calculated as

$$V_{Q1\_ds\_max}=V_{D1\_max}=|V_{\rm in}|_{\rm max}+V_{o1} \tag{20}$$

The maximum reverse voltage across the drain and the source terminals of $D_2$ in a half line cycle can be expressed as

$$V_{Q2\_ds\_max}=V_{o1\_max}\times\frac{N_2}{N_1}-V_{o2\_min}. \tag{21}$$

The maximum voltage across diode $D_2$ in a half line cycle can be expressed as

$$V_{D2\_max}=|V_{\rm in}|_{\rm max}\times\frac{N_2}{N_1}+V_{o2\_avg} \tag{22}$$

Under the condition $V_{in}=110$ Vrms, $N_1$:$N_2=8$:1, $V_{o1\_max}=49$ V, $V_{o1\_min}=47$ V, $V_{o2\_max}=3$ V, $V_{o2\_min}=1$ V, the maximum voltage across the drain to source terminals of $Q_1$ and the reverse voltage on $D_1$ are calculated to be 203 V, the reverse voltage across diode $Q_2$ is calculated to be 5.25 V, and the voltage across the drain to source terminals of $Q_2$ is calculated to be around 22 V.

The current stresses of these components in one switching cycle is summarized in Table II. The current stresses of these components cannot be calculated from the expression in Table II since the timespans ($t_1$–$t_0$) and ($t_3$-$t_2$) are unknown yet. Further derivation is needed to find the mathematical expressions for the component current stresses. The timespans ($t_1$–$t_0$), ($t_2$·$t_1$), ($t_3$-$t_2$), and ($t_4$-$t_3$) will also be derived.

To calculate the current stresses of these components, the time intervals ($t_1$–$t_0$) and ($t_3$-$t_2$) need to be calculated as well. In a half line cycle, the root-mean-square (rms) value of the time interval I input current $I_{in\_T1\_rms}$ can be expressed as

$$I_{ph1\_rms}=\frac{P_{ph1\_avg}}{V_{in\_rms}} \tag{23}$$

where (23) $P_{ph1\_avg}$ represents the average time interval I input power. The constant coefficient $k$ between the input voltage and the time interval I input current can be expressed as

$$k=\frac{I_{ph1\_avg}}{V_{\rm in}}. \tag{24}$$

Combining (10) and (24) yields

$$k=\frac{(t_1-t_0)^2}{2\times T_s\times L_{N1}}. \tag{25}$$

The coefficient $k$ can be also expressed as

$$k=\frac{I_{ph1\_rms}}{V_{in\_rms}}. \tag{26}$$

Combining (23), (25), and (26) yields

$$(t_1-t_0)=\frac{1}{V_{in\_rms}}\sqrt{2\times P_{ph1\_avg}\times T_s\times L_{N1}}. \tag{27}$$

Combining (8) and (27), the switching current in $Q_1$ at time $t_1$ can be expresses as

$$I_{Q1\_t1}=\frac{V_{in\_rec}}{V_{in\_rms}}\sqrt{\frac{2\times P_{ph1\_avg}\times T_s}{L_{N1}}}. \tag{28}$$

With the voltage–second balance law, one can also get

$$(t_2-t_1)=(t_1-t_0)\times\frac{V_{\rm in}}{V_{o1}}. \tag{29}$$

Substituting (27) into (29) yields

$$(t_2-t_1)=\frac{V_{in\_rec}}{V_{o1}}\times\frac{1}{V_{in\_rms}}\sqrt{2\times P_{ph1\_avg}\times T_s\times L_{N1}}. \tag{30}$$

The energy supplied from the ac input during the time interval II operation is equal to the energy delivered to the LED load via output $V_{o2}$ in every switching cycle. Therefore, the following relationship is valid:

$$\frac{1}{2}\times I_{D_2\_t_3}^2\times L_{N2}=P_{o2}\times T_s=I_{\rm LED}\times V_{o2}\times T_s. \tag{31}$$

Rearranging (31) yields

$$\begin{aligned}I_{D_2\_t_3}=I_{Q_2\_t_3}&=\sqrt{\frac{2\times I_{\rm LED}\times V_{o2}\times T_s}{L_{N2}}}\\&=\sqrt{\frac{2\times I_{\rm LED}\times V_{o2}\times T_s}{L_{N1}}}\left(\frac{N_1}{N_2}\right).\end{aligned} \tag{32}$$

The switching current reflects to the winding $N_1$ at time $t_3$ can, therefore, be written as

$$I_{N_1\_t_3} = I_{Q_1\_t_3} = \sqrt{\frac{2 \times I_{\rm LED} \times V_{o2} \times T_s}{L_{N1}}}. \quad (33)$$

Substituting (33) into (16) yields

$$(t_3 - t_2) = \frac{1}{V_{in\_rec}} \times \sqrt{2 \times I_{\rm LED} \times V_{o2} \times T_s \times L_{N1}}. \quad (34)$$

One should note that $V_{in\_rec} = 0$ should not be used to calculate ($t_3$-$t_2$) as the minimum value of $V_{in\_rec}$ is $V_{\rm aux}$. According to the voltage–second balance law, the time ($t_4$-$t_3$) can be expressed as

$$(t_4 - t_3) = (t_3 - t_2) \times \frac{V_{in\_rec}}{V_{o2}} \times \frac{N_2}{N_1}. \quad (35)$$

Substituting (34) into (35) yields

$$(t_4 - t_3) = \sqrt{\frac{2 \times I_{\rm LED} \times T_s \times L_{N1}}{V_{o2}}} \times \frac{N_2}{N_1}. \quad (36)$$

Although the switching current in $Q_1$ peaks at $t_1$ and $t_3$ in one switching cycle, it is found that the maximum current in $Q_1$ occurs at $t_1$ when $V_{in}$ is at the maximum in a half line cycle, which can be explained as follows. The square of $I_{Q1\_t1}$ is proportional to the time interval I input power and the square of $I_{Q1\_t3}$ is proportional to the time interval II input power. The maximum time interval I input power is far higher than the maximum of time interval II input power. Therefore, the maximum switching current in $Q_1$ occurs at $t_1$ of a switching cycle when the ac input voltage and the time interval I input power are also at their maximum.

By replacing $V_{in\_rec}$ with $V_{in\_rec\_max}$ in (28), the maximum peak switching current in $Q_1$ and $D_1$ is calculated to be 1.09 A under the condition $P_{ph1\_avg} = 7.5$ W, $V_{in\_rms} = 110$ Vrms, $N_1$:$N_2$ = 8:1, $L_{\rm N1} = 1.25$ mH, By replacing $V_{o2}$ with $V_{o2\_max}$ in (32), the maximum switching current in $Q_2$ and $D_2$ is calculated to be 1.51 A under the condition $V_{o2\_max} = 3$ V, $I_{\rm LED} = 0.15$ A, $N_1$:$N_2$ = 8:1, and $L_{\rm N1} = 1.25$ mH.

## IV. Control Scheme

Fig. 7 shows the control diagram of the proposed MRC LED driver. Two control loops are needed for the LED driver, namely, the LED current feedback loop and the output $V_{o2}$ voltage loop.

To achieve LED current regulation, the LED current is sensed and compared with its current reference. The compensated error signal, $V_{\rm ctrl1}$, is compared with the sawtooth signal to generate the gate driving signal for MOSFET $Q_1$ during the interval I operation. Under steady state, $V_{\rm ctrl1}$ is a constant in a half line cycle. Therefore, the ON time of $Q_1$ during phase one ($t_1$–$t_0$) is constant. Under discontinuous conduction mode and flyback topology, the interval I input current automatically follows the input voltage to perform the power factor correction [33]. When the sensed input current is not equal to the LED current reference, $V_{\rm ctrl1}$ will be changed automatically by the feedback loop. Therefore, ($t_1$–$t_0$) and the rms input current will change. The change in the rms input current lead to change in the input power and the output voltage $V_{o1}$. $V_{o1}$ will settle to the value

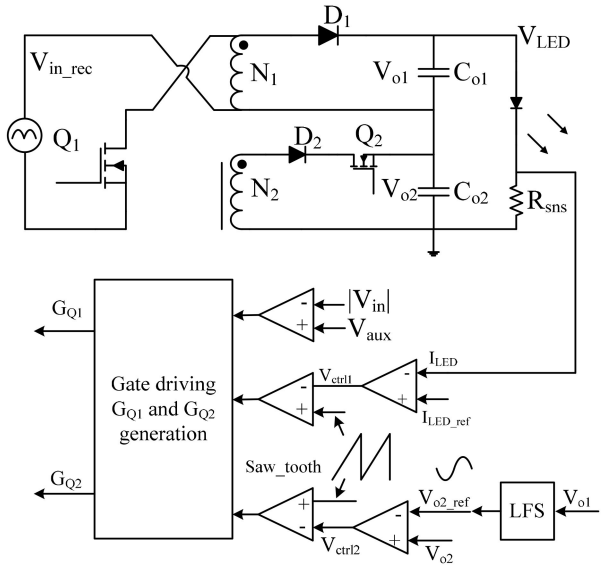


Fig. 7. Control diagram of the proposed MRC LED driver.

that produces the exact LED current required by its reference. It should be noted that the average voltage $V_{o2}$ is a constant, and it is not a part of the LED current regulation loop.

To achieve ripple cancellation, the output voltage $V_{o1}$ is sensed by the low-frequency sensing (LFS) circuit to extract the double-line-frequency ripple voltage. The sensed ripple voltage becomes the reference voltage of $V_{o2}$, $V_{o2\_ref}$. The output voltage $V_{o2}$ is sensed and compared with this reference. The compensated error voltage $V_{\rm ctrl2}$ is compared with the sawtooth signal to produce the gate driving signal of $Q_1$ during the interval II operation. The voltage loop used to regulate $V_{o2}$ should have a high enough bandwidth (>10 kHz) to achieve close tracking of the reference voltage. In the experimental prototype, a type II compensation with ~10 kHz bandwidth is used in the regulation loop for $V_{o2}$. There is also logic required to control the gate driving of $Q_1$. When $|V_{in}| < V_{\rm aux}$, the gate driving of $Q_1$ during the interval I operation is disabled. In this way, no energy is delivered to the output $V_{o1}$ during this period, minimizing the amount of energy going through two power conversion steps.

Fig. 8 shows how to generate the gate driving pulse for $Q_1$ and $Q_2$. The control signals $V_{\rm ctrl1}$ and $V_{\rm ctrl2}$ are compared with the same sawtooth signal to generate the gate driving $G_{Q1}$ and $G_{Q2}$ for $Q_1$ and $Q_2$. At time $t_0$, the beginning of a switching cycle, $Q_1$ is turned ON and the inductor current in winding $N_1$ starts increasing. At time $t_1$, the control signal $V_{\rm ctrl1}$ and the sawtooth signal crossover, which terminates the ON period of $G_{Q1}$. The inductor current starts decreasing and transferring energy to the output $V_{o1}$. At time $t_2$, the inductor current drops to zero, which triggers the turn-ON of $Q_1$ again. $Q_2$ is also turned ON at $t_2$. The inductor current in winding $N_1$ starts increasing again. At time $t_3$, the sawtooth signal and $V_{\rm ctrl2}$ crossover, which terminates the ON period of $Q_1$ for the second time. The inductor current in winding $N_1$ commutes to winding $N_2$ and starts decreasing and drops to zero at time $t_4$. Before the start of the next switching cycle, there is a small time interval [$t_4$–$t_5$] to maintain the DCM operation.

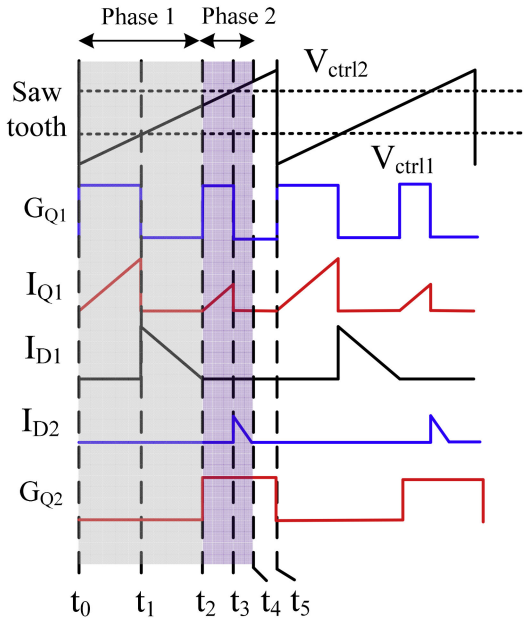


Fig. 8. Gate driving generating scheme for $Q_1$ and $Q_2$.

TABLE III
SIMULATED POWER FACTOR PERFORMANCE OF THE PROPOSED LED DRIVER UNDER 110 VRMS INPUT

| $V_{o1\_rip}$ / $V_{LED}$ | 5% | 10% | 20% | 30% | 40% |
|---|---|---|---|---|---|
| Power factor ($V_{aux}$ = 20 V) | 0.99 | 0.98 | 0.93 | 0.85 | 0.7 |
| Power factor ($V_{aux}$ = 30 V) | 0.99 | 0.99 | 0.96 | 0.90 | 0.78 |
| Power factor ($V_{aux}$ = 40 V) | 0.99 | 0.99 | 0.97 | 0.92 | 0.84 |
| Power factor ($V_{aux}$ = 50 V) | 0.99 | 0.99 | 0.97 | 0.94 | 0.88 |

## V. DESIGN CONSIDERATIONS AND EXAMPLE DESIGN PROCEDURES

In this section, the design considerations for the MRC LED driver will be discussed and an example design procedure will also be presented.

### A. $V_{o1}$ Ripple Versus Input Current Distortion

EnergyStar requires power factor implementation for LED drivers with greater than 5 W output. In the proposed design, the interval II input current introduces distortion, which inevitably affects the power factor performance. A model to simulate the average input current of the proposed LED driver has been built. The power factor performance simulation is based on 110 Vrms input, and the results are shown in Table III. To normalize the result, the voltage ripple of $V_{o1}$ is presented as the ratio of $V_{o1\_rip}/V_{\rm LED}$, where $V_{o1\_rip}$ is the ripple voltage amplitude of $V_{o1}$. Note that the dc amplitude of $V_{o2}$ $V_{o2\_dc}$ is designed based on the minimum requirement to be just enough to maintain $V_{o2}$ above zero. Therefore, in the proposed design, there is $V_{o2\_dc} = V_{o1\_rip} = V_{o2\_\rm rip}$. In this way, the average power delivered to $V_{o2}$ is minimized and so is the input current distortion. In a real design, $V_{o2\_dc}$ can be designed slightly higher than $V_{o1\_rip}$ to provide a reasonable margin.

As shown in Table III, the power factor of the proposed LED driver is reduced when the ripple ratio $V_{rip\_vo1}/V_{\rm LED}$ is increased. Under the same ripple ratio, the power factor is improved when $V_{\rm aux}$ is increased from 20 to 50 V. The improvement is not obvious when the ripple ratio is low, for example, when the ripple ratio $V_{o1\_rip}/V_{\rm LED}$ is 5% or 10%. The improvement becomes obvious when the ripple ratio is high. For example, when $V_{o1\_rip}/V_{\rm LED} = 40\%$, the power factor is improved from 0.7 when $V_{\rm aux} = 20$ V to 0.88 when $V_{\rm aux} = 50$ V.

In addition to the power factor requirement, IEC61000-3-2 class C sets limit on the input harmonic currents for lighting devices with greater than 75 W power. Two sources contribute to input current distortion, the ac input current during the interval II operation and the ac input current zero-crossing distortion caused by the addition of $V_{\rm aux}$. The input harmonic currents are simulated based on 110 Vrms input, 50 V, 1.5 A, 75 W output, and the results are presented in Figs. 9–11.

Fig. 9(a) shows the input harmonic currents with $V_{o1\_rip}/V_{\rm LED} = 5\%$ and $V_{\rm aux} = 20$ V. Each order of input harmonic current is well below the limit set by IEC-61000-3-2 class C. Fig. 9(b) shows the input harmonic currents when $V_{o1\_rip}/V_{\rm LED} = 10\%$. Each order of input harmonic current is still below the limit. However, the 21st- and 23rd-order input harmonic currents are already very close to the 3% limit. Fig. 9(c) shows the input harmonic currents when $V_{o1\_rip}/V_{\rm LED} = 20\%$. The input harmonic currents from the second interval input current contribute significantly to the overall harmonic current. As a result, multiple harmonic currents exceed the limit. Fig. 10(a) shows the input harmonic currents when $V_{\rm aux}$ is designed to be 30 V and $V_{o1\_rip}/V_{\rm LED} = 5\%$. Each order of input harmonic current is also very well below the limit. When $V_{\rm aux}$ is increased to 40 V and $V_{o1\_rip}/V_{\rm LED} = 5\%$, the 11th-order input harmonic current exceeds the 3% limit, as shown in Fig. 11(a). In this case, because of a higher $V_{\rm aux}$, the zero-crossing distortion is more severe and contributes significantly to the overall harmonic currents.

Input harmonic currents in Figs. 9(a) and 10(a) meet the requirement of IEC-61000-3-2 class C, while the results from other design parameters having harmonic currents exceeding the limit or too close to the limit without enough margin. In general, to reduce the input current harmonic currents, it is preferred to have a small $V_{o1\_rip}/V_{\rm LED}$ . The presence of voltage $V_{\rm aux}$ also introduces the zero-crossing distortion. When $V_{o1\_rip}/V_{\rm LED}$ is selected, $V_{\rm aux}$ should also carefully selected so that the harmonic currents from zero-crossing distortion do not contribute significantly to the input harmonic currents.

### B. $V_{o1}$ Ripple Versus Output Capacitor $C_{o1}$

The capacitor $C_{o1}$ serves as the storage capacitor to buffer the imbalanced energy between the ac input and the LED output in a half line cycle. The relationship between $C_{o1}$ and the ripple voltage of $V_{\rm o1}$ can be expressed as

$$C_{o1} = \frac{P_{\rm LED} \times T_{\rm line}}{2\pi \times V_{o1\_avg} \times V_{o1\_rip\_pp}}. \tag{37}$$

Equation (37) reveals that the capacitance of $C_{o1}$ is inversely proportioned to the peak-to-peak ripple voltage of $V_{o1}$. In other words, if a larger ripple voltage is allowed on $V_{o1}$, the storage

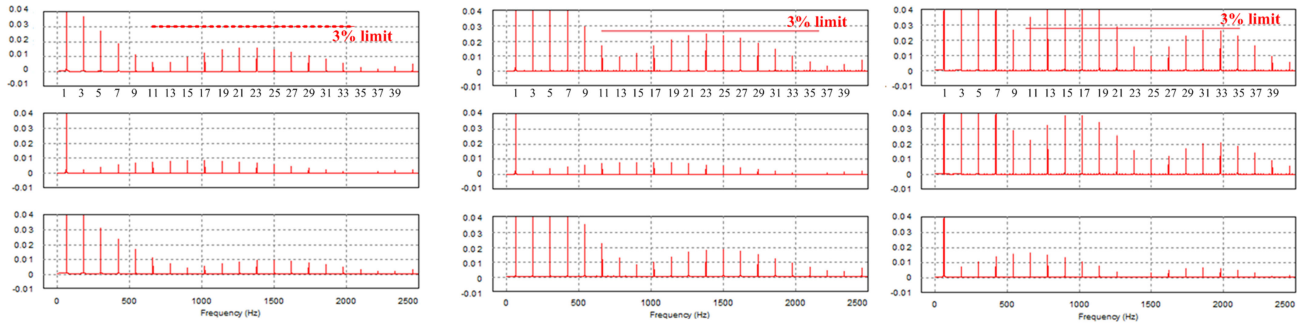


Fig. 9. Input harmonic currents when $V_{in} = 110$ Vrms, $V_{\rm LED} = 50$ V, $I_{\rm LED} = 1.5$ A, $V_{\rm aux} = 20$ V. (a) $V_{\rm aux} = 20, V_{o1\_rip}/V_{\rm LED} = 5\%$. (b) $V_{\rm aux} = 20, V_{o1\_rip}/V_{\rm LED} = 10\%$. (c) $V_{\rm aux} = 20, V_{o1\_rip}/V_{\rm LED} = 20\%$.

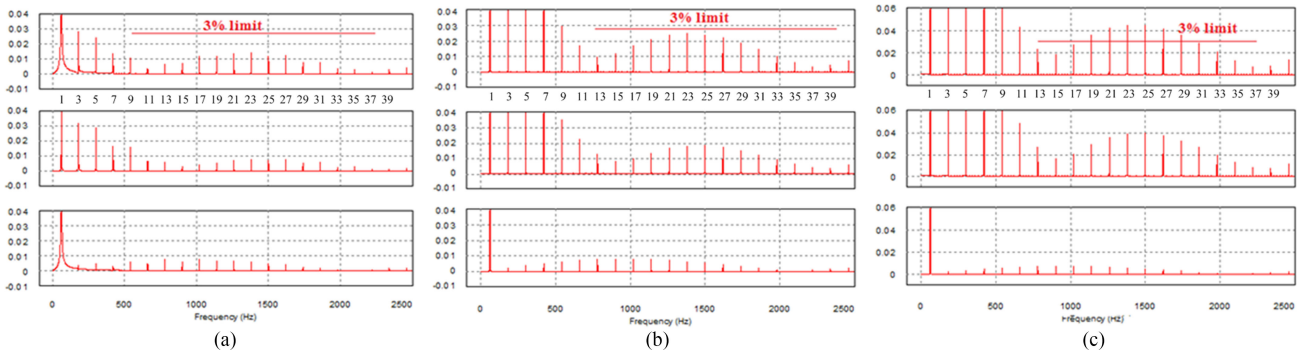


Fig. 10. Input harmonic currents when $V_{in} = 110$ Vrms, $V_{\rm LED} = 50$ V, $I_{\rm LED} = 1.5$ V, $V_{\rm aux} = 30$ V. (a) $V_{\rm aux} = 30, V_{o1\_rip}/V_{\rm LED} = 5\%$. (b) $V_{\rm aux} = 30, V_{o1\_rip}/V_{\rm LED} = 10\%$. (c) $V_{\rm aux} = 30, V_{o1\_rip}/V_{\rm LED} = 20\%$.

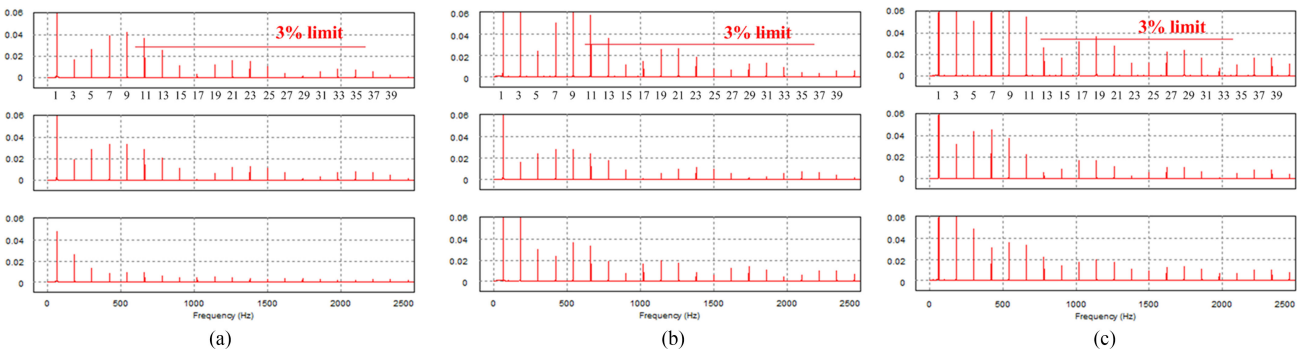


Fig. 11. Input harmonic currents when $V_{in} = 110$ Vrms, $V_{\rm LED} = 50$ V, $I_{\rm LED} = 1.5$ V, $V_{\rm aux} = 40$ V. (a) $V_{\rm aux} = 40, V_{o1\_rip}/V_{\rm LED} = 5\%$. (b) $V_{\rm aux} = 40, V_{o1\_rip}/V_{\rm LED} = 10\%$. (c) $V_{\rm aux} = 40, V_{o1\_rip}/V_{\rm LED} = 20\%$.

capacitor $C_{o1}$ can be smaller. A smaller storage capacitor is preferred in the LED driver design to reduce overall size and even achieve electrolytic capacitor-free design to extend system life. Because of ripple cancellation, flicker-free LED driving can always be achieved, even with a significant ripple voltage present on $V_{o1}$. Therefore, one of the objectives in the proposed LED driver design is to reduce the capacitor $C_{o1}$, which also means a large ripple voltage on $V_{o1}$. One should note that $V_{o1\_rip}$ is also linked to the input current distortion discussed earlier. For example, the power factor will be reduced when a larger ripple voltage is presented on $V_{o1}$. In addition, it will be discussed that the power conversion loss is also related to the ripple voltage, as will be discussed later. Design trade-offs on $V_{o1_rip}$should be made in order to achieve an overall optimized design.

### C. Output Capacitor $C_{o2}$

The capacitor $C_{o2}$ for the output $V_{o2}$ is used for filtering the switching frequency ripple. It is not required to store energy in a half line cycle. Therefore, a ceramic capacitor can be used in a design. A 22-μF ceramic capacitor is used in the experimental prototype.

TABLE IV
AMOUNT OF POWER THAT GOES THROUGH TWO TIMES POWER CONVERSION (PERCENTAGE OF THE TOTAL OUTPUT POWER)

| $V_{aux}$ | $V_{o1\_rip}$ / $V_{LED}$ | | | | |
|---|---|---|---|---|---|
| | 5% | 10% | 20% | 30% | 40% |
| 20 V | 0.03 W (0.4%) | 0.06 W (0.8%) | 0.14 W (1.8%) | 0.25 W (3.3%) | 0.46 W (6.1%) |
| 30 V | 0.04 W (0.5%) | 0.12 W (1.6%) | 0.21 W (2.8%) | 0.37 W (4.9%) | 0.66 W (8.8%) |
| 40 V | 0.06 W (0.8%) | 0.15 W (2%) | 0.27 W (3.6%) | 0.49 W (6.5%) | 0.85 W (11.3%) |
| 50 V | 0.08 W (1%) | 0.17 W (2.2%) | 0.36 W (4.8%) | 0.68 W (9%) | 1.04 W (13.8%) |

### D. $V_{o1}$ Ripple Versus Conversion Loss

As discussed earlier, it is preferred to have a large ripple voltage $V_{o1\_rip}$ to minimize the output capacitor $C_{o1}$. However, a large ripple voltage $V_{o1\_rip}$ will also reduce the power factor performance. To maintain a reasonably good power factor, $V_{\rm aux}$ should be increased along with $V_{o1\_rip}$. For example, as shown in Table III, the power factor is increased from 0.7, when $V_{\rm aux} =$ 20, to 0.88, when $V_{\rm aux} = 50$ V. Therefore, it can be understood that to maintain a high power factor, $V_{\rm aux}$ should be increased when a higher ripple voltage $V_{o1\_rip}$ is to be allowed in the proposed design.

When $V_{\rm aux}$ is not active, the energy is delivered from the ac input directly to output $V_{o1}$ and $V_{o2}$, respectively. Therefore, this part of energy only goes through one-time power conversion. On the other side, when $V_{\rm aux}$ is active, the energy provided to $V_{o2}$ is processed twice, from the ac input to $V_{\rm aux}$ first and then from $V_{\rm aux}$ to $V_{o2}$.

The amount of energy provided by $V_{\rm aux}$ to $V_{o2}$ is related to both the ripple voltages $V_{o1}$ and $V_{\rm aux}$, as indicated by (7). A larger $V_{\rm aux}$ will lead to a longer timespan that $V_{\rm aux}$ is active. At the same time, a larger ripple $V_{o1}$ means a larger $V_{o2\_avg}$. Therefore, more energy will be transferred from $V_{\rm aux}$ to $V_{o2}$ and more energy goes through two power conversion steps. The amount of power being processed twice is calculated, and the result is shown in Table IV, under 110 Vrms input, 7.5 W output with different $V_{o1\_rip}/V_{\rm LED}$ and $V_{\rm aux}$.

As shown in Table IV, to reduce the amount of energy being processed twice to maintain high efficiency, the ripple voltage of $V_{o1}$ should be reduced. Therefore, multiple design considerations are related to $V_{o1\_rip}$ and design trade-offs are necessary.

On the other side, the amount of power going through two times power conversion is much higher in the previous ripple cancellation LED drivers, in which the percentage of power that must be processed twice is directly proportional to the ripple ratio $V_{o1\_rip}/V_{\rm LED}$ . For example, a 30% $V_{o1\_rip}/V_{\rm LED}$ in the previous ripple cancellation LED driver means 30% output power goes through two times power conversion. The amount of energy going through two times power conversion is much less in this new proposed LED driver when $V_{o1\_rip}/V_{\rm LED}$ is 30%. For example, as shown in Table IV, when $V_{\rm aux} = 30\%$, the amount of power being processed twice is 4.6% of the total output power while 0.9 power factor can still be achieved under this arrangement, as shown in Table III.

### E. Selection of $C_{\rm aux}$

As discussed in Section II, (5) can be used to calculate the energy supplied by $V_{\rm aux}$. $C_{\rm aux}$ can be selected based on the voltage change on $V_{\rm aux}$ when it supplies energy to the LED load. The relationship between $C_{\rm aux}$, $E_{\rm aux}$, $V_{\rm aux,}$ and the voltage change on $V_{\rm aux}$ $\Delta V_{\rm aux}$ can be expressed as

$$E_{\rm aux} = \frac{1}{2}C_{\rm aux}V_{\rm aux}^2 - \frac{1}{2}C_{\rm aux}(V_{\rm aux} - \Delta V_{\rm aux})^2 \tag{38}$$

where $\triangle V_{\rm aux}$ represents the voltage drop on $V_{\rm aux}$ when it supplied energy to the output. Rearranging (38) yields

$$C_{\rm aux} = \frac{2E_{\rm aux}}{V_{\rm aux}^2 - (V_{\rm aux} - \Delta V_{\rm aux})^2}. \tag{39}$$

Under the condition $V_{\rm aux} = 30$ V, $V_{in} = 110$ Vrms, $V_{o2\_avg} =$ 2.5 V, and $I_{\rm LED} = 0.15$ A, $E_{\rm aux}$ is calculated to be 0.3 mJ by (5). Using (39) and assuming $\Delta V_{\rm aux} = 2$ V, the capacitor $C_{\rm aux}$ is calculated to be 5.2 μF.

### F. Maintain DCM Operation

DCM operation is needed to ensure interval I input current follows the input voltage. In other words, [$t_0$–$t_4$] should be smaller than the predefined switching period $T_s$. Since the expressions of ($t_1$–$t_0$), ($t_2$-$t_1$), ($t_3$-$t_2$), and ($t_4$-$t_3$) have been derived, the total time ($t_4$–$t_0$) can be expressed as

$$\begin{aligned}(t_4 - t_0) &= (t_1 - t_0) + (t_2 - t_1) + (t_3 - t_2) + (t_4 - t_3)\\ &= \frac{1}{V_{in\_rms}}\sqrt{2 \times P_{in\_avg} \times T_s \times L_{N1}} + \frac{V_{in\_rec}}{V_{o1}}\\ &\quad \times \frac{1}{V_{in\_rms}}\sqrt{2 \times P_{\rm in\_avg} \times T_s \times L_{N1}}\\ &\quad + \frac{1}{V_{in\_rec}} \times \sqrt{2 \times I_{\rm LED} \times V_{o2} \times T_s \times L_{N1}}\\ &\quad + \sqrt{\frac{2 \times I_{\rm LED} \times T_s \times L_{N1}}{V_{o2}}} \times \frac{N_2}{N_1}.\end{aligned} \tag{40}$$

Equation (40) is only valid when $T_s > (t_4$–$t_0)$, and this should be verified for a proposed design. With known $P_{in\_avg}$, $T_s$, $L_{N1}$, $V_{in\_rms}$, $I_{\rm LED}$, $V_{o1}$, $V_{o2}$, and $N_2$:$N_1$, the time ($t_4$–$t_0$) can be calculated and plotted in a half line cycle. An ideal $(t_4$–$t_0)_{\rm max}$ should be just slightly smaller than $T_s$. For example, $(t_4$–$t_0)_{\rm max} = 48$ μs and $T_{\rm s} = 50$ μs. In this way, DCM operation can be maintained all the time and the component current stresses are minimized. Further adjusting $(t_4$–$t_0)_{\rm max}$ can be achieved by changing $L_{N1}$ as ($t_4$–$t_0$) is proportional to the square root of $L_{N1}$.

### G. Example Design Procedure

An example design procedure is presented as follows:

*Step 1:* Select the switching frequency. To reduce switching loss, it is preferred to reduce the switching frequency for low-power designs. Twenty kilohertz switching frequency can be selected to minimize switching loss while avoiding audible switching noise.

*Step 2:* Select the output capacitor $C_{o1}$. On one side, it is desirable to reduce the storage capacitor to minimize the

size of LED drivers and even achieving electrolytic capacitor-less designs. On the other side, a smaller $C_{o1}$ will lead to a higher voltage ripple $V_{o1\_rip}$, which further leads to a higher input current distortion and more conversion loss. Therefore, design trade-offs on selecting $C_{o1}$ should be made to achieve an overall optimized design. In particular, for higher than 75 W output power design, IEC 61000-3-2 class C sets the limit for input harmonic currents. It is more critical to select $C_{o1}$ to meet the input harmonic current requirement than to reduce capacitor size.

*Step 3:* Select the voltage $V_{\rm aux}$. For less than 75 W output power designs, the power factor performance is one of the major concerns. A higher $V_{\rm aux}$ can be used to improve the power factor correction performance. For higher than 75 W output power designs, the presence of $V_{\rm aux}$ also contributes to the input harmonic currents. A higher $V_{\rm aux}$ does not necessarily reduce the input harmonics current and can even lead to increased input current harmonics. $V_{\rm aux}$ should be selected to achieve an overall minimal harmonic current. Fig. 12 shows an example of input harmonic currents under different $V_{\rm aux}$. In Fig. 12(a), because $V_{\rm aux}$ is small, the interval II input current dominates the harmonic contents. In Fig. 12(c), with a high $V_{\rm aux,}$ the zero-crossing distortion harmonics dominant. Comparing the results in Fig. 12(a), (b), and (c), Fig. 12(b) presents the best result, with each order of harmonic current far below the limit. If no $V_{\rm aux}$ can be found to meet the IEC-61000-3-2 class C requirement, it is an indication that $V_{o1\_rip}$ is too large in the design. In this way, one needs to go back to step 2 to select a larger $C_{o1}$ to reduce $V_{o1\_rip}$.

*Step 4:* Select the turns ratio $N_1$:$N_2$. As shown in Tables I and II, the voltage and current stresses of $Q_2$ and $D_2$ are closely related to the turns ratio $N_1$:$N_2$. In addition, (14) places one more restriction on the turns ratio, which is $N_1$:$N_2 < V_{\rm o1}$:$V_{\rm o2}$. In the experimental prototype, $N_1$:$N_2 = 8$:1 is selected to keep the voltage stresses of $Q_2$ and $D_2$ being around 20 V. In this way, low-voltage-rating components can be selected for $D_2$ and $Q_2$.

*Step 5:* Select the inductance $L_{N1}$. To maintain DCM operation, $L_{N1}$ should be selected to make $(t_4{-}t_0)_{\max}$ smaller than $T_s$. At the same time, it is desirable to have a larger $L_{N1}$. As indicated in (28) and (32), a larger $L_{N1}$ reduces the current stresses of $Q_1$, $D_1$, $Q_2$, and $D_2$. In the experimental prototype, $L_{N1}$ is designed to be 1.25 mH.

*Step 6:* Final parameter adjustment. Steps 4 and 5 can be repeated for a few iterations until a satisfying set of parameters is obtained.

## VI. Comparison Between Different LED Driving Technologies

In this section, a comparison between different LED driving technologies will be made and the result is summarized in Table V.

A conventional single-stage LED driver can achieve high efficiency since only one power conversion step is required. The other advantages of conventional single-stage LED drivers include low cost, low-input harmonic currents, and high power factor. However, it is very difficult, almost impossible, to achieve flicker-free LED driving performance. The output ripple voltage of a single-stage LED driver, which is caused by the imbalanced energy between input and output, is applied to the LED load directly and produces significant ripple LED current, which causes lighting flicker. Large storage capacitors are also required by a single-stage LED driver to buffer the imbalanced energy between the ac input and the dc LED output.

A conventional two-stage LED driver can achieve flicker-free LED driving, high power factor, and low-input harmonic currents. The first stage performs power factor correction while the second-stage regulates the LED current. However, due to two stages of power conversion, the component cost is high and the efficiency is relatively low.

The previous ripple cancellation LED driver can achieve flicker-free LED driving, high power factor, and low-input harmonic currents. The amount of power that goes through two times power conversion is related to the voltage amplitude of the ripple cancellation voltage. The efficiency of a ripple cancellation LED driver is between the efficiency of a single-stage LED driver and a two-stage LED drive. There is a small extra cost to build the ripple cancellation converter. The required storage capacitor for a previous ripple cancellation LED driver is much lower than a single-stage LED driver.

The proposed multiplexing ripple cancellation LED driver can achieve high efficiency and flicker-free LED driving. The unique operation distorts the input current from its ideal form. However, an optimized design can be achieved with significantly reduced storage capacitor, reasonably good power factor performance, and high efficiency.

## VII. Experimental Verifications

To verify the proposed MRC LED driver, a 7.5-W experimental prototype was designed based on the procedure presented in previous section, built, and tested. Table VI gives the design specification and the circuit parameter of the experimental prototype.

Fig. 13 shows the ripple cancellation waveforms of the proposed MRC LED driver. The double-line-frequency ripple voltage on the output $V_{o1}$ is 2 V peak to peak. Due to grounding requirement, $-V_{o2}$ is measured in Fig. 13 instead of $V_{o2}$. The output $-V_{o2}$ has an in phase ripple voltage to cancel the ripple voltage from $V_{o1}$. In this way, the double-line-frequency ripple voltage on the LED is greatly reduced. The double-line-frequency ripple LED current is measured to be 16 mA peak to peak, which means 8 mA peak and the ripple current is 5.3% of the average LED current. Note that the occasional spikes on the LED current are excluded in the measurement. There are also noticeable voltage spikes on $V_{o2}$ caused by noise. The noisy natural of buck–boost operation introduced significant noise, which disturbs the voltage regulation loop of $V_{o2}$. The voltage spikes can be reduced or eliminated when a better layout is designed.

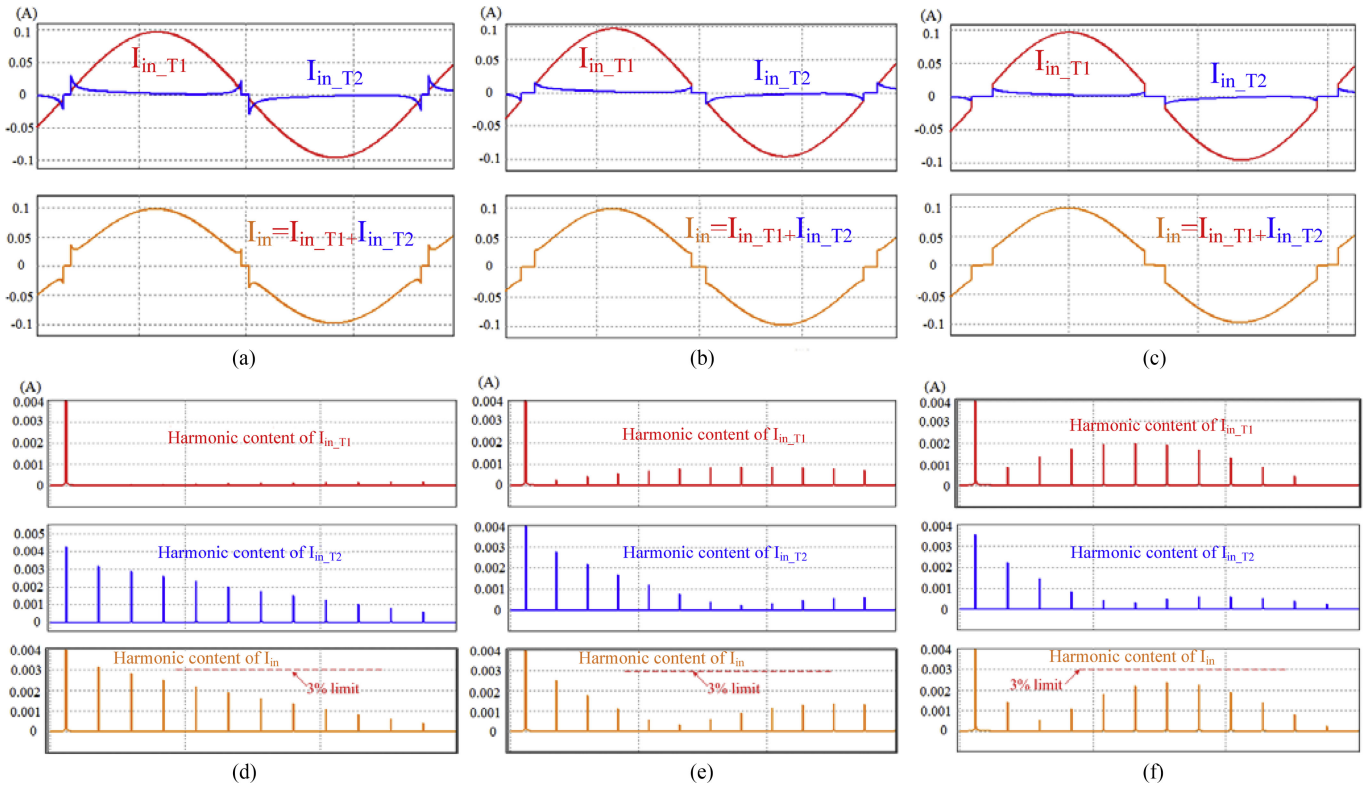


Fig. 12. Simulated harmonic input current of the proposed MRC LED driver under different $V_{\rm aux}$ ($V_{in}$ = 110 Vrms, $V_{o2\_min}$ = 0.5 V, $V_{o2\_max}$ = 2.5 V, $V_{\rm LED}$ = 50 V, $I_{\rm LED}$ = 0.15 A, $P_{\rm out}$ = 7.5 W). (1a) $V_{\rm aux}$ = 10V. (2a) $V_{\rm aux}$ = 20V. (3a) $V_{\rm aux}$ = 30V. (1b) $V_{\rm aux}$ = 10V. (1b) $V_{\rm aux}$ = 20V. (1c) $V_{\rm aux}$ = 30V.

TABLE V
COMPARISON BETWEEN DIFFERENT LED DRIVING TECHNOLOGIES

| Topology | Power processed | Efficiency | Required storage capacitor | Flicker-free LED driving | Power factor performance | Input harmonic currents | Cost |
|---|---|---|---|---|---|---|---|
| Single-stage LED driver | 100% output power is processed one time | High | High. | No | High | Low | Low |
| Two-stage LED driver | 100% output power is processed two times | Low | High | Yes | High | Low | High |
| Previous ripple cancellation LED driver | 90% output power is processed one time and 10% output power is processed two times (when $V_{o1\_rip}$ / $V_{\rm LED}$ = 10%) | Intermediate to high | Low | Yes | High | Low | Intermediate |
| Proposed multiplexing ripple cancellation LED driver | 99.2% output power is processed one time and 0.8% output power is processed twice ($V_{o1\_rip}$ / $V_{\rm LED}$ = 10% and $V_{\rm aux}$ = 20 V) | High | Low | Yes | Intermediate to high | Intermediate | Intermediate |

Fig. 14 shows the gate driving and the switching current waveforms of the MRC LED driver. A switching cycle starts at time $t_0$ when MOSFET $Q_1$ is turned ON. The magnetic current in winding $N_1$ (and $Q_1$) starts rising from zero. The magnetic current peaks at $t_1$ when $Q_1$ is turned OFF, and it continues flowing in $D_1$. The magnetic current drops to zero before the time $t_2$, which ends the interval I operation. MOSFET $Q_1$ is turned ON at $t_2$ again and the magnetic current in winding $N_1$ starts increasing from zero again. The current peaks at $t_3$ when $Q_1$ is turned OFF. The magnetic current then commutes from winding $N_1$ to winding $N_2$ and continues its flow in diode $D_2$ and MOSFET $Q_2$. The current in winding $N_2$ drops to zero at time $t_4$, which ends the interval II operation.

Fig. 15 shows the voltage stresses of $Q_1$, $Q_2$, and $D_2$ in the experimental prototype. The input current waveform and the output voltage waveforms are also included to reflect the full-load operating condition. The maximum voltage of $Q_1$ is around 190 V. The voltage stresses of $Q_1$ in the LED driver is the same as it is in a conventional buck–boost LED driver. The voltage across the anode of diode $D_2$ and the source of $Q_2$ is measured. When the voltage is positive, it indicates $D_2$ is forward biased while the body diode of $Q_2$ is reversely biased. Vice versa, it

TABLE VI
DESIGN SPECIFICATION AND CIRCUIT PARAMETER

| **Design specification** | |
|---|---|
| Input voltage | 89 Vrms – 132 Vrms |
| $V_{LED}$ | ~ 50 V |
| $I_{LED}$ | 0.15 A |
| **Circuit parameter** | |
| Coupled inductor | $N_1$: $N_2$ = 8:1, $L_{N1}$=1.25 mH EE16 core |
| Main MOSFET $Q_1$ | 2SK2803 (450 V 3 A) |
| Main output diode $D_1$ | LQA06T300 (300 V 6 A) |
| MOSFET $Q_2$ | ZXMN4A06GTA (40 V 5 A) |
| Output diode $D_2$ | MBRS340T3G (40 V 4 A) |
| Capacitor $C_{aux}$ | ECA-1HM470B (47 µF, 50 V) |
| Output capacitor $C_{o1}$ | EKZE101ELL271MK30S (270 µF, 100 V) |
| Output capacitor $C_{o2}$ | CL21A226KOQNNNE (22 µF, 16 V) |
| LED current sensing resistor | KNP100JR-73-0R5 (0.5 ohm) |
| Controller | PIC16F1578-I/SS |
| Switching frequency $f_s$ | 20 kHz |

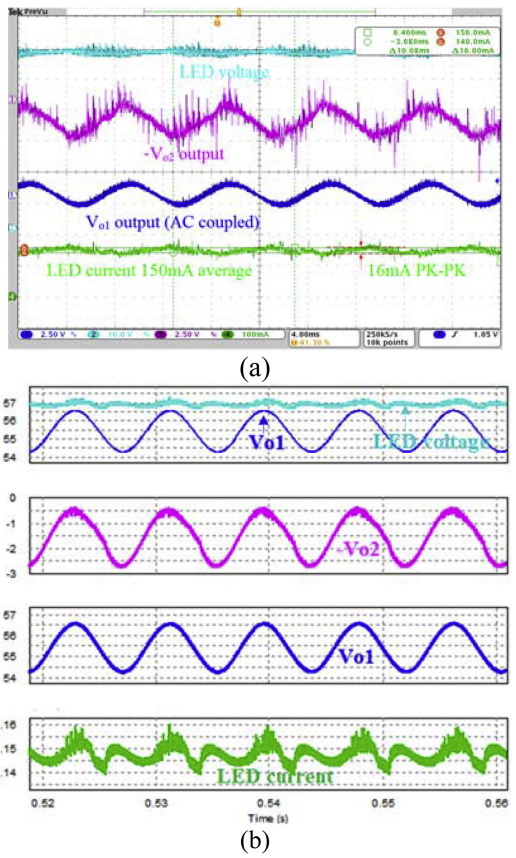


Fig. 13. Ripple cancellation waveforms of the proposed MRC LED driver: (a) experimental result and (b) simulated result with the PSIM 11.0 version.

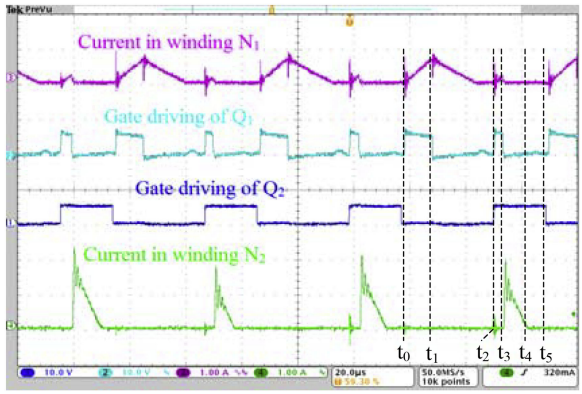


Fig. 14. Key switching waveform of the MRC LED driver.

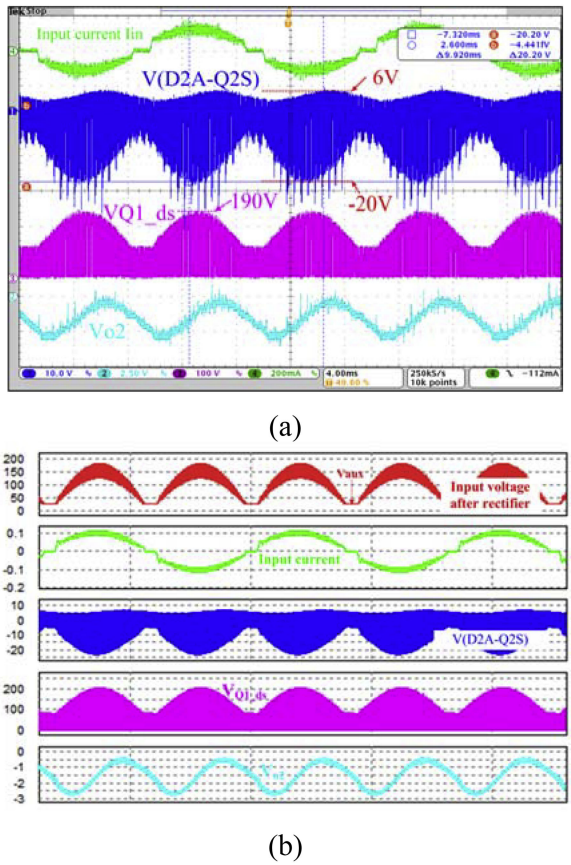


Fig. 15. Power components voltage stresses of the MRC LED driver: (a) measured result and (b) simulated result with PSIM 11.0 version.

indicates $D_2$ is reversely biased while the body diode of $Q_2$ is forward biased. Therefore, as shown in Fig. 15, the maximum voltage on $D_2$ is around 6 V while the maximum voltage on $Q_2$ is around 20 V.

Fig. 16 shows the efficiency of the proposed MRC LED driver with and the efficiency of a conventional single-stage buck–boost LED driver. The efficiency of MRC prototype is 1% lower than the efficiency of a conventional LED driver. This is due to extra switching loss with the second interval operation. Overall, this is a very small price to pay when flicker-free LED driving

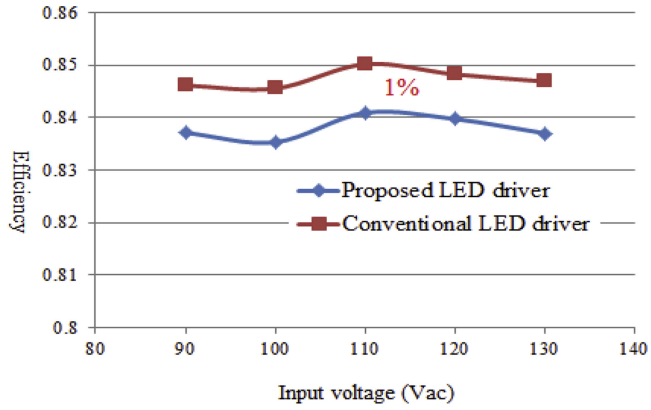


Fig. 16. Efficiency of the experimental prototype LED driver with/without RCU under full-load condition (red line: without RCU; blue line: with RCU).

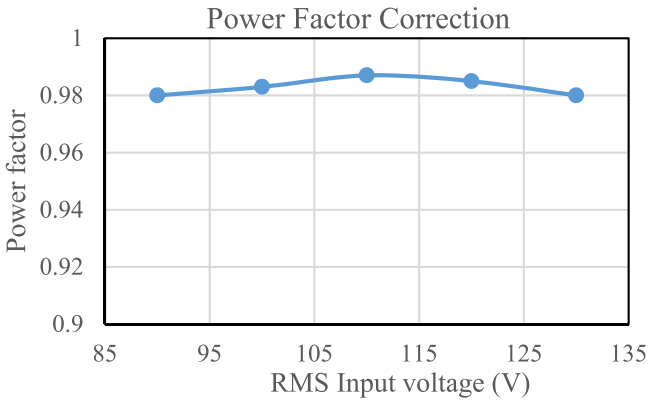


Fig. 17. Power factor correction performance of the MRC LED driver.

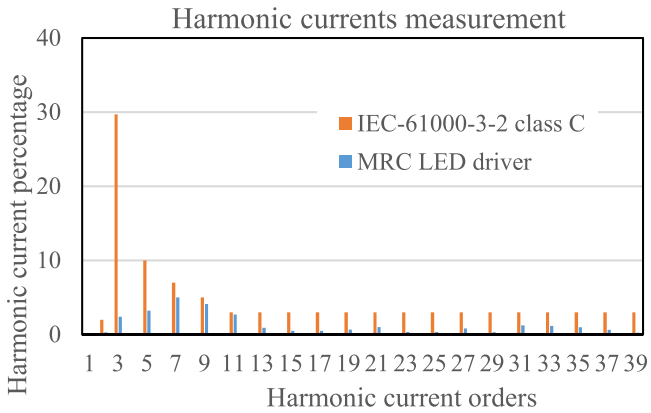


Fig. 18. Input current harmonics of the proposed MRC LED driver under 110 Vrms input.

performance is achieved. On the other hand, to achieve flicker-free LED driving performance and the same efficiency with a two-stage LED driver, the second-stage dc–dc converter needs to achieve 99% efficiency, which is not realistic to achieve with a conventional design. Assuming the second-stage buck converter achieves 95% efficiency, the final efficiency of the two-stage LED driver will be $85\% \times 0.95 = 80.7\%$, which is significantly lower than the proposed LED driver.

Fig. 17 shows the power factor correction performance of the proposed MRC LED driver. Around 0.98 PF has been achieved under full load condition. Fig. 18 shows the input current harmonics of the proposed LED driver. The experimental results show that the converter is able to meet the requirements outlined by IEC 61000 3 2 class C, however, the 9th- and 11th-order harmonic currents are very close to the limit. It is expected that the input current harmonics can be further reduced with an optimized input filter design.

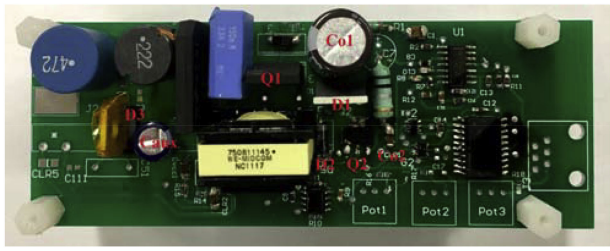


Fig. 19. 7.5-W MRC LED driver experimental prototype.

Fig. 19 shows the photo of the experimental prototype.

## VIII. Conclusion

In this paper, an MRC LED driver is proposed to achieve flicker-free LED driving, high efficiency, and a high power factor correction. The power circuit is operated in time multiplexing manner with two intervals in one switching cycle. The operation in interval I performs power factor correction and transfers energy from the ac input to the LED load. The operation in interval II produced the opposite ripple voltage to achieve ripple cancellation. The proposed MRC LED driver also achieves true single-stage power conversion, improving efficiency over previous ripple cancellation LED driver. One sacrifice of achieving single-stage power conversion is an increased input harmonic current. With a proper design parameter, the input current harmonics can be limited to meet the requirement of IEC-61000-3-2 class C. The LED driver can maintain a low cost by minimizing additional components, making it a very competitive solution for cost-sensitive low-power designs. A 7.5 W experimental prototype had been built and tested to verify the operation of the LED driver. The experimental prototype achieves 0.98 PF, 5.3% of double-line-frequency ripple LED current performance while the efficiency is only 1% efficiency lower than a conventional buck–boost LED driver.

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